SONY

CXD2565M

1-bit D/A Converter for Audio (with Built-in DF)

Description

The CXD2565M is a 1-bit stereo D/A converter developed specifically for CD players. This IC incorporates an 8-times oversampling digital filter. (Master clock: 768fs)

Characteristics

Digital filter section

- Ripple: 0.002dB or less
- Attenuation: –75dB or more

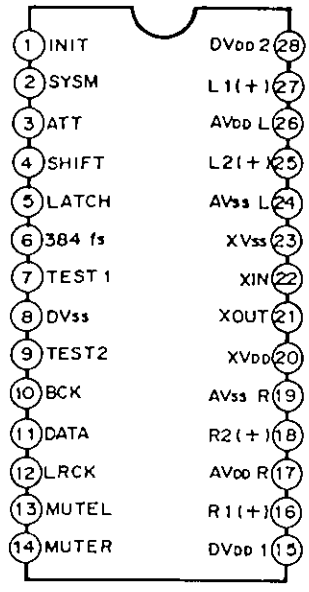
DAC section

- Dynamic range: 116dB (theoretical value)
- S/N ratio: 96dB or more
- Distortion: 0.004% or less

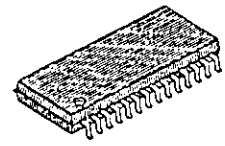
Features

- Master clock: 768fs
- Sony's original, new 3rd-order noise shaper
- PLM pulse conversion output (complementary PLM)
- Direct digital sync
- Selectable input word length: 18 or 16bits

Pin Configuration (Top View)



28 pin SOP (Plastic)



Structure

Silicon gate CMOS IC

Applications

CD players, CD-I players

Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.5 to 6.5	V
• Input voltage	V_I	–0.3 to V_{DD}+0.3	V
• Allowable power dissipation			
	P_D (Ta=60 °C)	500	mW
• Storage temperature			
	Tstg	–55 to 150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature			
	Ta	–10 to 60	°C
• OSC frequency	Fx (768fs)	24.0 to 37.0	MHz

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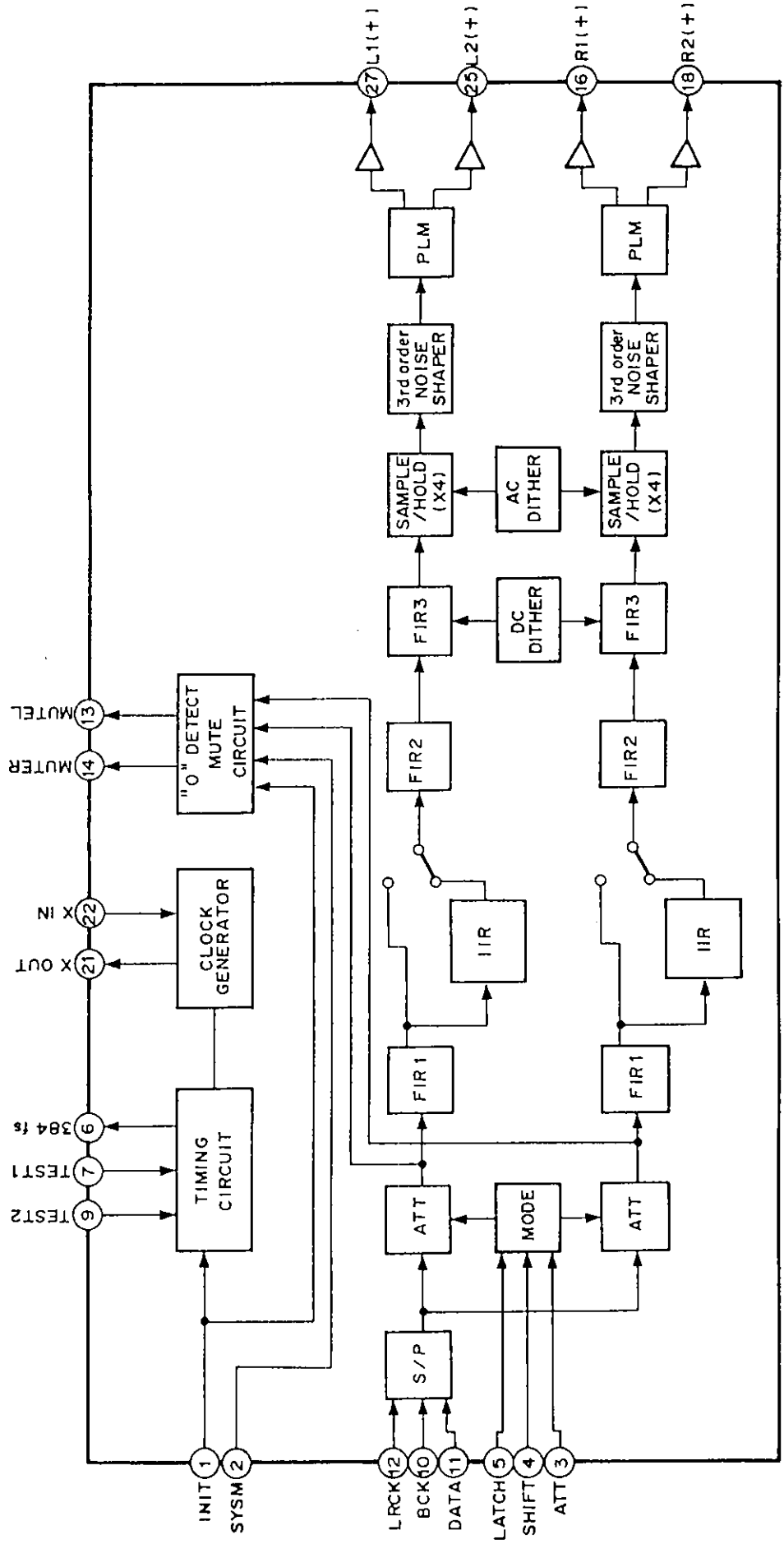
Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	INIT	I	Resynchronized on the rising edge of this signal
2	SYSM	I	System mute input
3	ATT	I	Serial control data input
4	SHIFT	I	Shift clock input
5	LATCH	I	Latch clock input
6	384fs	O	384 fs clock output
7	TEST1	I	Test pin; normally fixed to Low
8	DVss	——	Digital GND
9	TEST2	I	Test pin; normally fixed to Low
10	BCK	I	BCK input
11	DATA	I	Data input
12	LRCK	I	LRCK input
13	MUTEL	O	Lch mute flag output
14	MUTER	O	Rch mute flag output
15	$DV_{DD}1$	——	Digital power supply
16	R1 (+)	O	Rch PLM output 1 (positive phase)
17	$AV_{DD}R$	——	Rch analog power supply
18	R2 (+)	O	Rch PLM output 2 (positive phase)
19	AVssR	——	Rch analog GND
20	XV_{DD}	——	Master clock power supply
21	XOUT	O	Crystal oscillator output pin (768 fs)
22	XIN	I	Crystal oscillator input pin (768 fs)
23	XVss	——	Master clock GND
24	AVssL	——	Lch analog GND
25	L2 (+)	O	Lch PLM output 2 (positive phase)
26	$AV_{DD}L$	——	Lch analog power supply
27	L1 (+)	O	Lch PLM output 1 (positive phase)
28	$DV_{DD}2$	——	Digital power supply

Electrical Characteristics

DC Characteristics

(DV_{DD}=XV_{DD}=$AV_{DD}R$=$AV_{DD}L$=5.0V ± 5%, DVss=XVss=AVssL=AVssR=0V, Ta=–10 to 60°C)

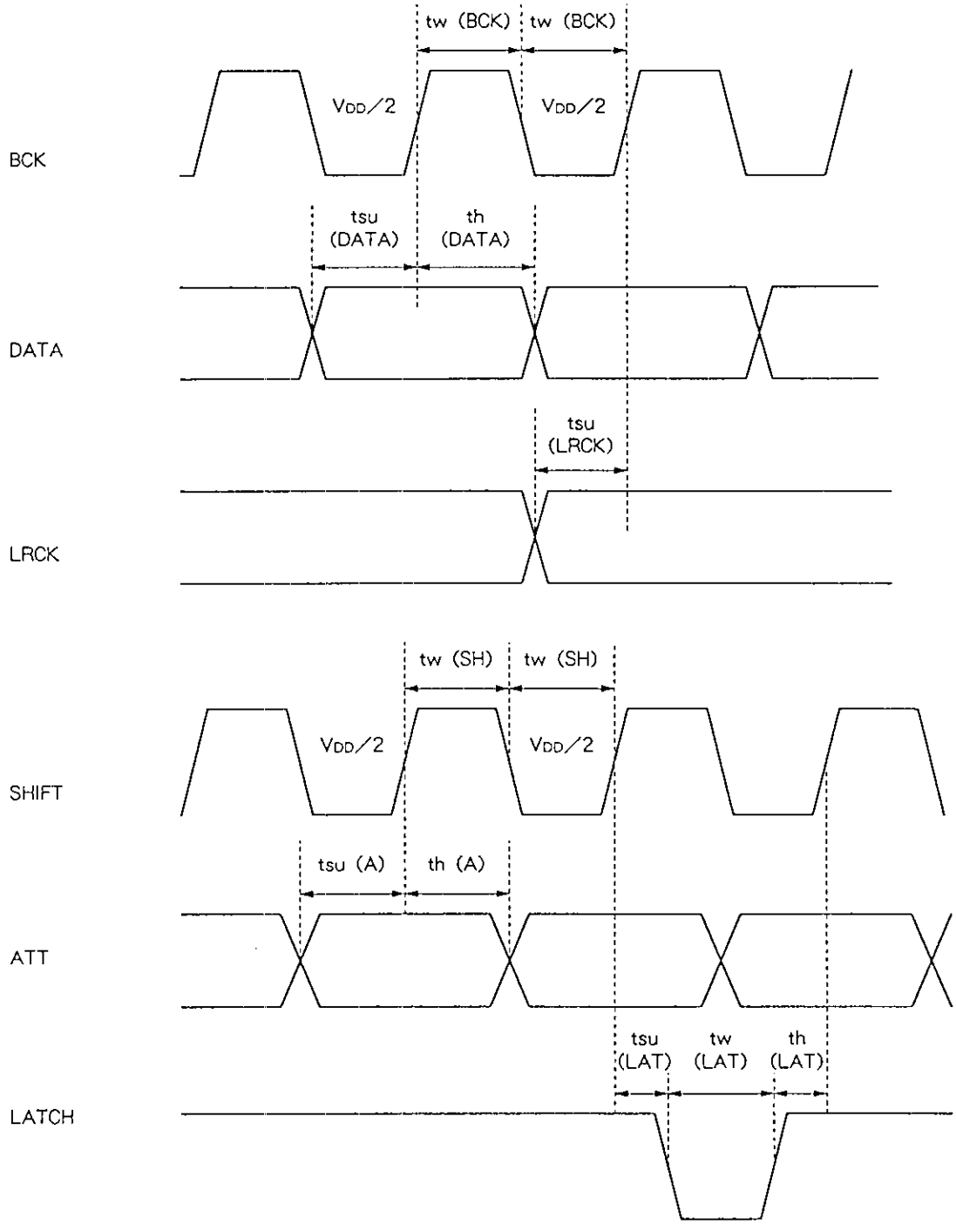
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High voltage	XIN	V_{IHX}		0.90V_{DD}			V
	Others	V_{IH}		0.76V_{DD}			V
Input Low voltage	XIN	V_{ILX}				0.10V_{DD}	V
	Others	V_{IL}				0.24V_{DD}	V
Input leakage current		I_I		–5.0		5.0	µA
Output High voltage	384fs	V_{OH}	Io=–0.4mA	V_{DD}–0.5			V
	R1, R2 (+) L1, L2 (+)	V_{OHA}	Io=–12mA	V_{DD}–0.5			V
	XOUT	V_{OHX}	Io=–1.2mA	V_{DD}–0.5			V
	MUTEL, MUTER	V_{OHM}	Io=–1.0mA	V_{DD}–0.5			V
Output Low voltage	384fs	V_{OL}	Io=0.4mA			0.4	V
	R1, R2 (+) L1, L2 (+)	V_{OLA}	Io=12mA			0.5	V
	XOUT	V_{OLX}	Io=1.2mA			0.5	V
	MUTEL, MUTER	V_{OLM}	Io=1.0mA			0.4	V
Current consumption		I_{DD}			20	60	mA

AC Characteristics

(DV_{DD}=XV_{DD}=$AV_{DD}R$=$AV_{DD}L$=5.0V ± 5%, DVss=XVss=AVssL=AVssR=0V, Ta=–10 to 60°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
BCK pulse width	tw (BCK)		156			nsec
DATA setup time	tsu (DATA)		20			nsec
DATA hold time	th (DATA)		20			nsec
LRCK setup time	tsu (LRCK)		50			nsec
XIN duty cycle	duty (XIN)	V_{DD}/2 at 33MHz		50		%
SHIFT pulse width	tw (SH)		100			nsec
ATT setup time	tsu (A)		20			nsec
ATT hold time	th (A)		20			nsec
LATCH setup time	tsu (LAT)		18	20		nsec
LATCH hold time	th (LAT)		100			nsec
LATCH pulse width	tw (LAT)		100			nsec

Input/AC Timing



Analog Characteristics (DVDD=XVDD=AVDDR=AVDDL=5.0V, DVSS=XVSS=AVSSL=AVSSR=0V, Ta=25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total higher harmonic distortion	THD+N	Input data 1kHz, 0dB (Fs=44.1kHz)		0.0030	0.0040	%
S/N ratio	S/N	Input data 1kHz, 0/– ∞ 0dB (Fs=44.1kHz)	96			dB

Description of Functions

1. Mute function

(1) Zero-data detection
This detection is executed after attenuation processing.
- A zero-detection flag is output when consecutive conditions are kept where the upper 14bits of the input data are all 0 or 1 and the other lowerbits are DC.
- The detection period can be selected from 60ms or 300ms by serial control.
- The digital filter continues operating normally even while the zero-detection flag is output.

(2) Digital filter mute (D/F MUTE)
- This mute is activated at High in the ATT mode of serial control.
- The output from the D/F section is set to "0+DC offset."
- The internal operation of the digital filter operates normally.

(3) Noise shaper mute (NS MUTE)
- This mute is activated if any of the following conditions is met at High in the system mode of serial control:
  - When the zero-detection flag is set.
  - When High (=mute) is input to the input pin SYSM.
  - When the D/F MUTE flag is set.
- The noise shaper output is switched to an output with the DC offset component added in the D/F section.
- The internal operation of the noise shaper is kept operating. When the mute is cleared, the output is switched to that of the noise shaper immediately.

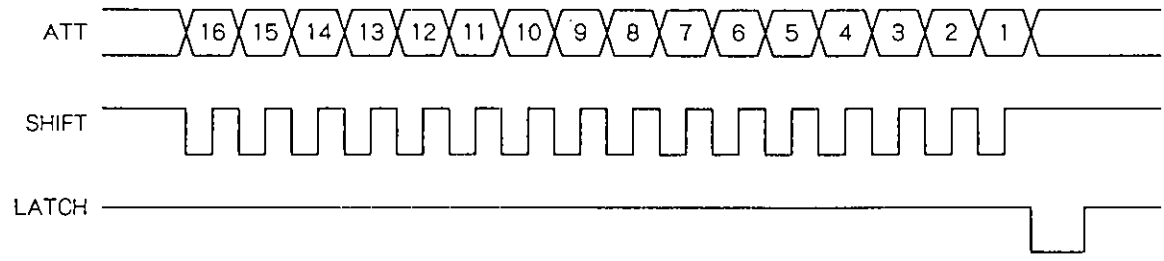
(4) INIT Low mute
- The input data of the D/F section is set to 0.
- The internal RAM is cleared.
- The output of the D/F section is set to "0+DC offset."
  (Before internal INIT after internal RAM cleared)
- After the internal INIT is pulled Low, the registers in the noise shaper section including the prehold section are cleared, with the output set to a 50% duty PWM (equivalent to 0).

2. Mute flag output (MUTEL, MUTER pins)

- If any of the following conditions is met, mute active flags are output from MUTEL and MUTER pins:
  (Flag polarities can be selected by serial control.)
  - When the zero-detection flag is set.
  - When High (=mute) is input to the input pin SYSM.
  - When the D/F MUTE flag is set.
  - When an external INIT is activated.

3. Serial control

- The mode is set by transferring mode data to the ATT, SHIFT, and LATCH pins.
- The transfer format is shown below.



- The data in bit 1 is always 0.
- The attenuate mode is entered when the data in bit 2 is 0.
  The system mode is entered when the data in bit 2 is 1.
- These settings are performed after an external INIT is cleared.
  (See the next page for details on mode setup.)

* SYNC function

- When SYNC is set to High in the system mode of serial control, resynchronization is executed once time after the rising edge of SYNC.
- 4 fs period (min.) or 5 fs period (max.) is required until the internal logic is synchronized.

Serial Control

• Attenuate mode

Bit	Mode flag	Function	High	Low
1	MODE1	MODE switching	Test mode	Normal mode
2	MODE2	MODE switching	System mode	Attenuate mode
3	EMP	De-emphasis	ON	OFF
4	MUTE	0+DC offset output	ON	OFF
5	ATT1	Attenuate data (MSB)		
6	ATT2	Attenuate data		
7	ATT3	Attenuate data		
8	ATT4	Attenuate data		
9	ATT5	Attenuate data		
10	ATT6	Attenuate data		
11	ATT7	Attenuate data		
12	ATT8	Attenuate data		
13	ATT9	Attenuate data		
14	ATT10	Attenuate data		
15	ATT11	Attenuate data		
16	ATT12	Attenuate data (LSB)		

* When INIT is Low, the MODE1, MODE2, EMP, and MUTE are reset to Low and ATT is set to 400H.

• System mode

Bit	Mode flag	Function	High	Low
1	MODE1	MODE switching	Test mode	Normal mode
2	MODE2	MODE switching	System mode	Attenuate mode
3	IFORM	Input data format	LSB first	MSB first
4	IBIT	Input data word length	18bits	16bits
5			don't care	
6			don't care	
7			don't care	
8	TEST1	Test mode setting	Normally fixed to Low	
9	TEST2	Test mode setting	Normally fixed to Low	
10	NS	Noise shaping	don't care	
11	MT1	Zero-data detection period	60ms	300ms
12	MT2	Zero-mute flag polarity	Muted when High.	Muted when Low.
13	FS32	Selection of de-emphasis fs	* See the table below	
14	FS48	Selection of de-emphasis fs	* See the table below	
15	SYNC	Input/output synchronization	ON	OFF
16	NSMUTE	NS mute function	ON	OFF

* When INIT is Low, all flags are reset to Low.
* Selection of de-emphasis fs

		32.0k	44.1k	48.0k	37.8k
13	FS32	High	Low	Low	High
14	FS48	High	Low	High	Low

4. INIT function

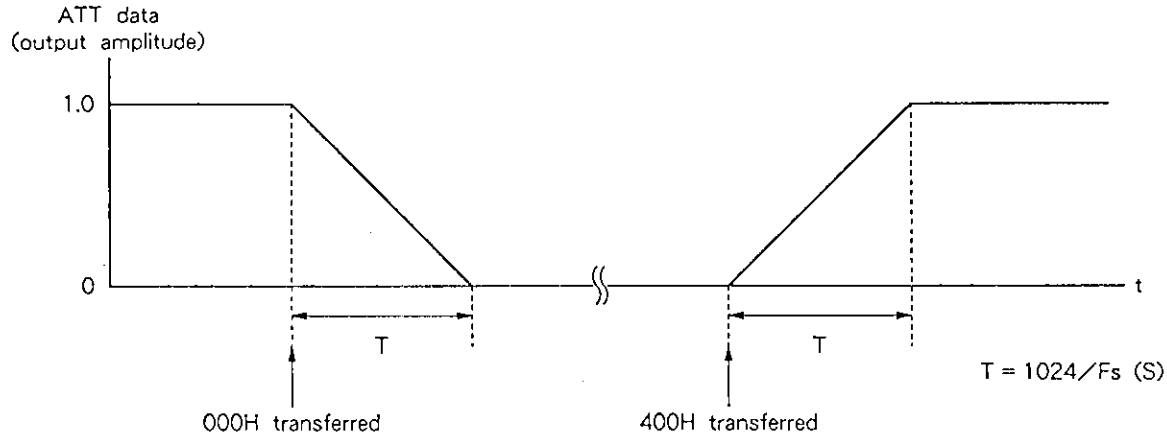
- The D/F and the NS sections are simultaneously cleared of reset immediately when resynchronization is executed after the rising edge of external INIT signal.
- External LRCK is not varied by the external INIT signal, so that the internal LRCK has its phase matched to the first external LRCK after the rising edge of external INIT signal by master clock level.
- 4 fs period (min.) or 5 fs period (max.) is required until the internal logic is synchronized.
- Internal INIT is delayed approximately 2 to 2.5ms after the falling edge of external INIT signal.

5. Double speed operation

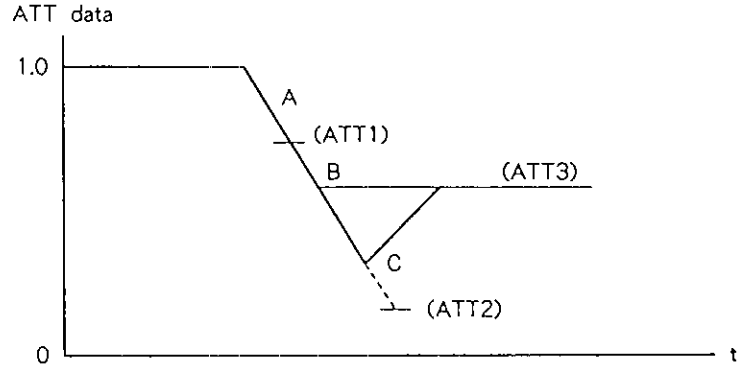
- The internal operations are performed at normal speed, maintaining synchronization for signals input in double speed.

6. Attenuator

- The ATT data is transferred using 12bits from bit 5 (MSB) to bit 16 (LSB). The amplitude of the data is 000H (0.0) to 400H (1.0).
  When INIT is Low, 400H is set as the ATT data.

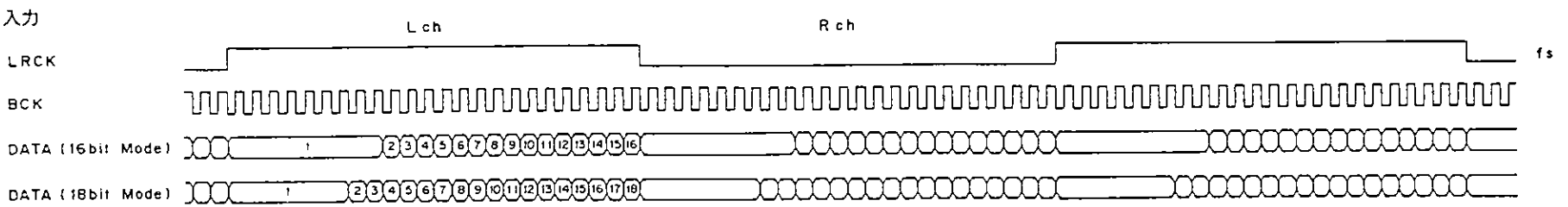


Soft muting is accomplished by transferring 000H as ATT. To clear, the ATT data immediately before the soft muting is applied (400H in the above case) is transferred.



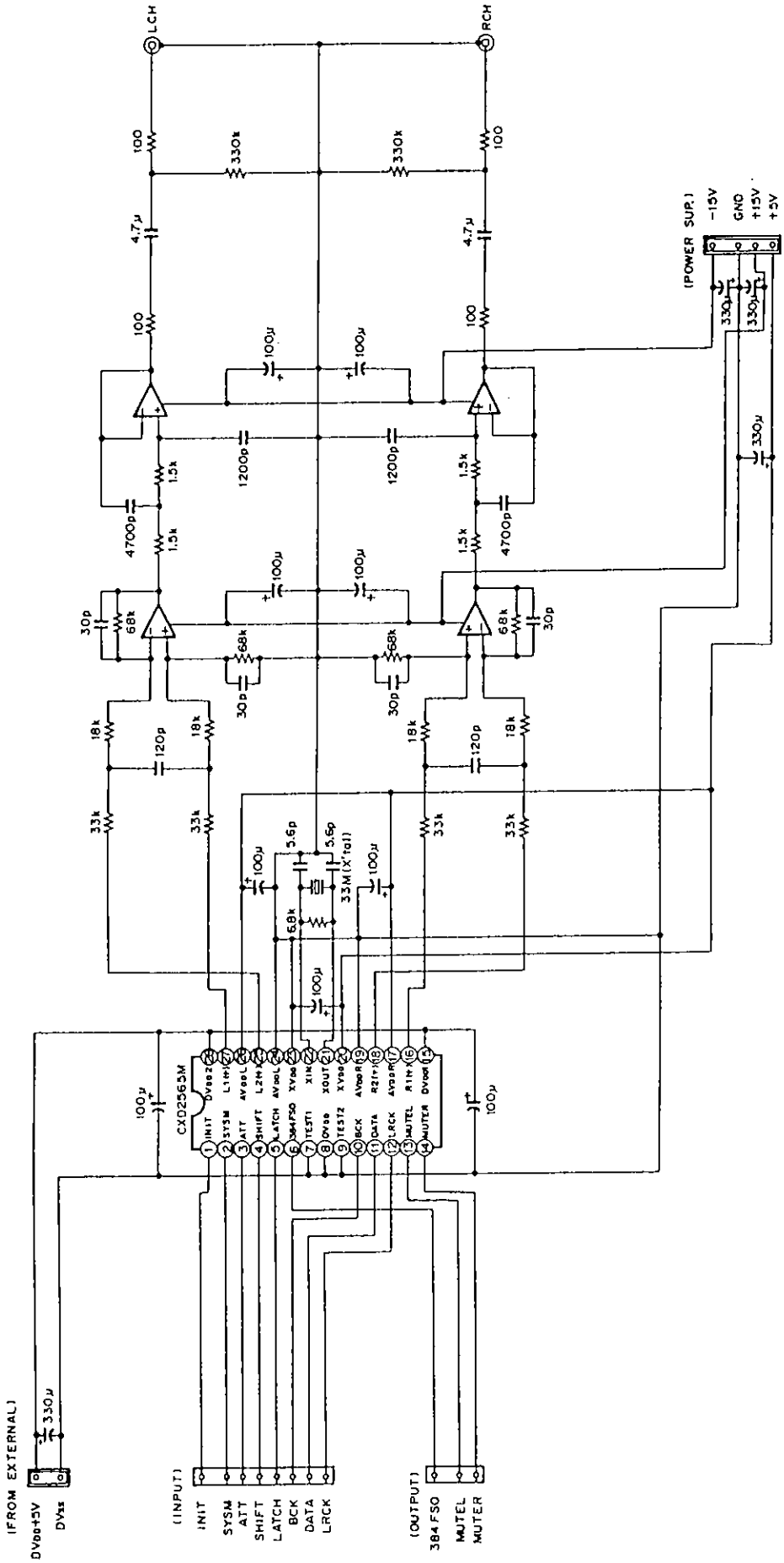
Thus, transition to new ATT data is always performed via soft muting operation. Assume that ATT1 followed by ATT2 is transferred, considering ATT1>ATT3>ATT2. If ATT2 is transferred before the value of ATT1 is reached (state A in the diagram), ATT1 is ignored and attenuation goes on approaching toward the value of ATT2. Next, ATT2 followed by ATT3 is transferred before the value of ATT2 is reached (B or C in the above diagram), ATT2 is ignored and attenuation goes on approaching toward the value of ATT3.

Data Input Timing



Input
* This is an example for the 24BCK/LSB first.

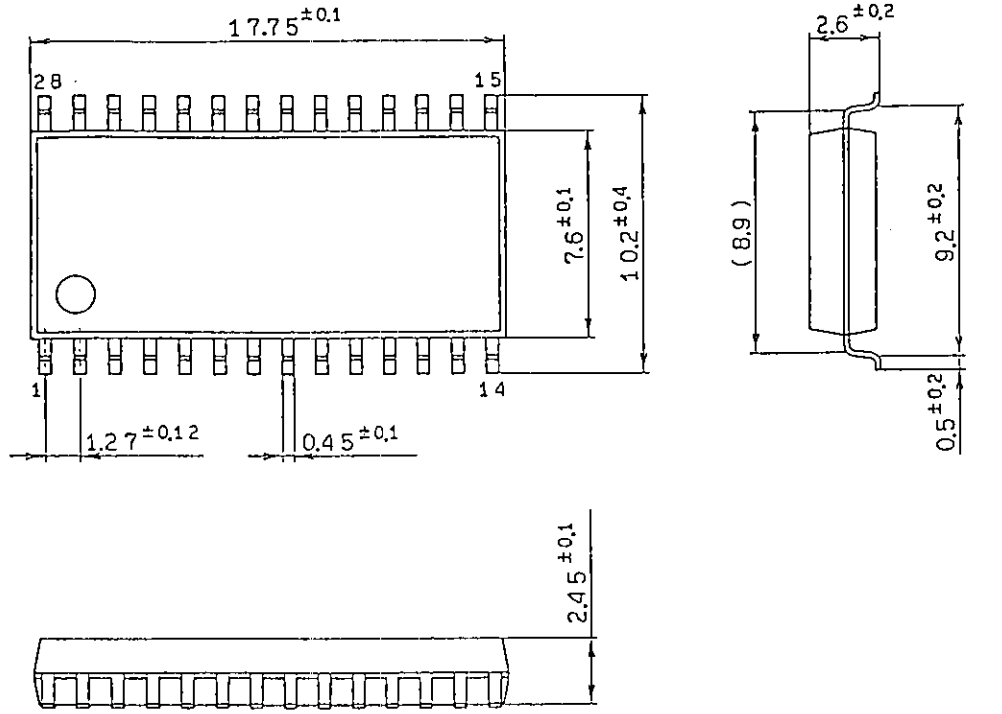
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

28pin SOP (Plastic) 375mil



SONY NAME	SOP-28P-L121
EIAJ NAME	*SOP028-P-0300-AX
JEDEC CODE	———